ATHARVA EDUCATIONAL TRUST'S
ATHARVA COLLEGE OF ENGINEERING
(Approved by AICTE, Recognized by Government of Maharashtra
& Affiliated to University of Mumbai - Estd. 1999 - 2000)

Department of Electronics & Telecommunication Engineering

Report on

One Day VLSI Webinar on

"RTL Design and Functional Verification"

Dated :10th August 2018 **Organised By**: EXTC Department

Schedule: 11am to 2pm

Venue:EXTC department, AtharvaCollege of Engineering, AtharvaEducational Complex, MaladMarve Road, charkop Naka, Malad(W), Mumbai 400095

Coordinators:Prof.MahalaxmiPalinje, Prof. Ritu Sharma, Prof. Susan Tony

Details of the Speaker:

Sr. No.	Name of the Speaker	Industry	Designation	Session	Audience	Venue
1.	Mr.Shivakumar	Maven Silicon	PR-Founder and CEO of Maven Silicon	11 am to 2pm	TE Students	EXTC Department Atharva College of Engineering

Objective of the Webinar:

1. To encourage and create awareness among the students about current needs in the VLSI industry
2. To give the students valuable insight about RTL designing in VLSI

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Workshop Coordinator	**(H.O.D, EXTC)**	**Principal, ACE.**
Prof Mahalaxmin Palinje	Prof. Jyoti Kolap	Dr. Shrikant Kallurkar
Prof Ritu Sharma		
Prof Susan Tony		

Address :Malad-Marve Road, Charkop Naka, Malad (W), Mumbai 400095, Maharashtra, India