

ATHARVA EDUCATIONAL TRUST'S

ATHARVA COLLEGE OF ENGINEERING

(Approved by AICTE, Recognized by Government of Maharashtra & Affiliated to University of Mumbai - Estd. 1999 - 2000)

Department of Electronics and Telecommunication

Report on

Two Day Workshop on

"Laboratory Experimentation with Electric: Open Source EDA System for VLSI Design"

Dated: 4th August 2017.

Organised by: EXTC Department

Schedule: 9am to 5pm

Venue: 4th Floor, Lab 5, ELEC DEPT, Atharva College of Engineering, Atharva Education

complex, Malad Marve Road, Charkop Naka, Malad (W), Mumbai 400095

Coordinators: Mahalaxmi Palinje

DETAILS OF SPEAKER:

Sr. No.	Name of Speaker	Industry	Designation	Session	Audience	Venue
1.	Janhavi Kulkarni	Eduvance	Lead Product Developer, gradeME	11.00am - 5.00pm	TE ET1&ET2 (EXTC) students	Lab No. 5 (ELEC), Phase 1, Atharva College of Engineering.
2.	Hardi Desai	Eduvance	Product Engineer, gradeME			

Objective of the workshop:

- 1) To encourage and create awareness among the students in the field of VLSI Design.
- To bridge gap between industry and Institute in designing Multimillion gate digital circuits using open source EDA: Electric Software.
- 3) The workshop also aims to introduce use of automatic evaluation platforms i.e GRADE ME in VLSI
- To understand impact of automatic evaluation on student learning.
- 5) Hands on practice on Electric software and grade ME platform

Workshop Committee Prof. Mahalaxmi Palinje Prof. Ritu Sharma

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H.O.D (EXTC) Prof. Jyoti Kølap

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