

TE sem IV C scheme summer 2025

(3 Hours)

[Total Marks: 80]

N.B.: (1) Question No. 1 is **Compulsory**.

(2) Attempt any **three** questions out of the remaining **five**.

(3) Each question carries 20 marks and sub-question carry equal marks.

(4) Assume suitable data if required.

5/6/25

EC5

- Q1 Attempt any Four (20)
- (a) Draw and explain a typical Instruction Cycle in a processor. (5)
 - (b) Explain Superscalar Architecture (5)
 - (c) What is Virtual Memory? (5)
 - (d) Define terms Speedup, Efficiency, Throughput related to pipeline (5)
 - (e) Compare CPU and GPU (5)
- Q2 (a) Explain Register Organization in CPU. (10)
- (b) Explain Segmentation and Paging mechanism (10)
- Q3. (a) Explain FIFO page replacement algorithm. Find out Miss ratio, Hit ratio for the following string using FIFO method. (Consider page frame size = 3) (10)
- 4, 7, 6, 1, 7, 6, 1, 2, 7, 2
- (b) Explain multicore processor Architecture in detail. (10)
- Q4 (a) What is deadlock condition in OS? (10)
- (b) Explain priority scheduling algorithm. For the given Priority Scheduling find average waiting time. (10)

Process	Arrival Time	Execution Time	Priority	Service Time
P0	0	5	1	0
P1	1	3	2	11
P2	2	8	1	14
P3	3	6	3	5

- Q5 (a) Describe Flynn's classification in detail. (10)
- (b) Explain Hardwired Control Unit in detail. Discuss any one method to implement it. (10)
- Q6 Write short note on (20)
1. Deadlock avoidance and prevention.
 2. Cluster
 3. Interprocess Communication.
 4. Pipeline hazards.
