T SEM III Choice based R-19 'C' Scheme ECS

6.6.25

(3 Hours) [Total Marks: 80]

N.B.: (1) Question No. 1 is **Compulsory**.
(2) Attempt any **three** questions out of the remaining **five**.
(3) Each question carries 20 marks and sub-question carry equal marks.
(4) Assume suitable data if required.

1. (a) Convert
i) $(9DB2)_{16}$ into binary.
ii) $(67.4A)_{16}$ into octal .
iii) $(37)_{10}$ to XS-3
iv) $(4C8.2)_{16}$ into Decimal
v)(1101) Gray to Binary **(5)**

(b) Implement Full adder using 8 :1 Multiplexer. **(5)**

(c) Design 2:1 Mux using IC 74153 **(5)**

(d) Explain full subtractor with truth table,k-map and logic diagram **(5)**

2. (a) Design and implement 7490 Pin diagram and as decade counter **(10)**

(b) Differentiate between Mealy and Moore machine **(10)**

3. (a) Implement the following function using PAL. F=Σ m=(0,3,4,7) and F2==Σ m=(1,2,5,7) **(10)**

(b) Implement Full Adder using PLA circuit. **(10)**

4. (a) Compare CPLD and FPGA devices. **(10)**

(b) Implement and explain 4-bit BCD adder using IC 7483. **(10)**

5. (a) Solve using K-map and implement same using logic gates
f(ABCD)= Σ m (4,5,7,12,14,15) + Σ d (3,8,10) **(10)**

(b) Reduce using Boolean Algebra Rules (x'yz + xy'z+xyz+xyz') and realize using AOI logic **(10)**

6. (a) Explain working of IC 74194 design it as ring counter **(10)**

(b) Design MOD 6 counter using MOD 8 counter. **(10)**