ATHARVA EDUCATIONAL TRUST'S

ATHARVA COLLEGE OF ENGINEERING

(Approved by AICTE, Recognized by Government of Maharashtra & Affiliated to University of Mumbai - Estd. 1999 - 2000)

Department of Electronics and Telecommunication

Report on
One week STC for Faculty on
"ICT based Online Program on VLSI DESIGN"

Dated : 14th to 18th March 2017

Organised by : EXTC Department

Time : 9.30 am to 4.00 pm

Speaker's Name: Dr. Rajesh Mehra, (NITTTR Chandigarh)

Venue : 2nd Floor, Lab 2, Atharva College of Engineering, Atharva Education complex , Malad Marve Road , Charkop Naka , Malad (W), Mumbai 400095

Coordinators : Divya Sharma / Varun Mishra

Targeted Audience : Faculties of Atharva College of Engineering

About the Workshop :

1) Learn & Interact with Experienced Faculties.

2) Basic knowledge on VLSI Design.

3) Participants understood working of various software.

4) Participants were encouraged to think and come up with new application ideas.

5) Interactive lecture sessions.

6) Group discussions to encourage innovation in the domain of VLSI.

No. of participants: 23

Day 1- Overview of VLSI by Dr. Rajesh Mehra and Device Simulation by Er. Amit Saini.

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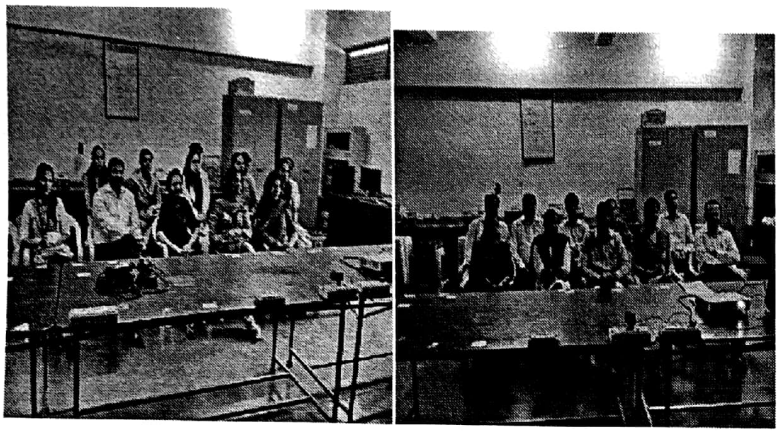
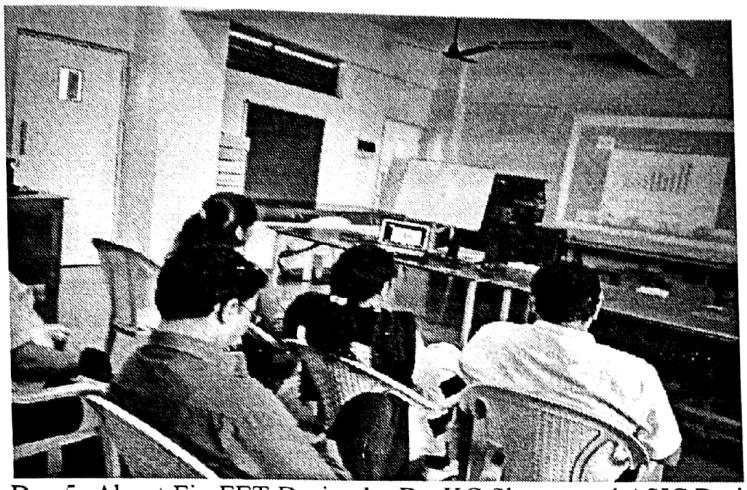


Day 2-Description of CAD Tools, Logic Optimization by Dr. Rajesh Mehra and Digital Design Simulation by Er. Uday K. SE.

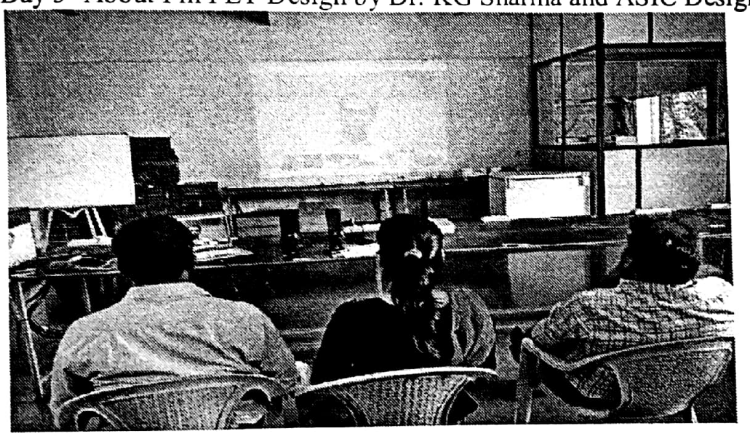
Day 3-About CMOS Design, Anolog CMOS Design by Er. H S Jatana and Analog Design Simulation by Er. Deep Sehgal.

Address : Malad-Marve Road, Charkop Naka, Malad (W), Mumbai 400095, Maharashtra, India

Day 4- About Advanced MOSFET, Chip Design by Er. H S Jatana and VLSI Issues & Challenges by Dr. KG Sharma.



Day 5- About Fin FET Design by Dr. KG Sharma and ASIC Design by Shallu Sharma.



Head of Department: Prof. Jyoti Kolap