[Max Marks 80] **[Time: 3hours]**

1) Question no. 1 is compulsory
2) Solve any three from the remaining five questions.
3) Assume suitable additional data if necessary.

Q1) Answer the following questions: (20)
a) Explain the significance of HOLD, RESET and READY signals in 8086 processor
b) List the steps taken by 8086 processor in response to receiving an interrupt.
c) Draw the 8086-8087 interfacing circuit representation in maximum mode of operation.
d) Explain the use & advantage of pipelining feature in 8086 architecture.

Q2) a) List and explain with examples memory addressing modes in 8086 processor. (10)
b) Explain the register structure of 8086 processor. (10)

Q3) a) With the help of memory map interface the following to an 8086 based system operating in minimum mode: (10)
i) 32K bytes of EPROM memory using 8k byte devices.
ii) 32K bytes of RAM memory using 8k byte devices.

b) Classify and explain 8086 instruction set. (10)

Q4) a) Explain the significance of flags and flag register of 8086 processor. (10)
b) Explain the need for DMA and modes of DMA data transfer typically made use of by the DMA controller IC - 8237. (10)

Q5) a) Explain the Intel Pentium processor's pipelining and superscalar architecture. (10)
b) With the help of a neat flowchart/algorithm write a program in 8086 assembly to copy an array of 100 numbers initialised in the data segment to extra segment. Assume additional data if any. (10)

Q6) Write short notes on: [ANY TWO]
a) Programmable interrupt controller – 8259. (10)
b) Intel Pentium processor – Branch Prediction Logic (10)
c) Programmable peripheral interface – 8255. (10)
d) INT 21H – DOS interrupt. (10)