

(Time: 3 Hours)

[Total Marks: 80]

- N.B.: (1) Question No. 1 is **compulsory**.
 (2) Solve any **three** questions out of remaining **five**.
 (3) Figures to **right** indicate **full** marks.
 (4) Assume suitable **data** where **necessary**.

- Q1. Solve any four 20
- Explain DC operating point and its variation with the help of output characteristics of transistor.
 - Convert S-R flip flop to J-K flip flop.
 - Design Ex-OR gate using NAND and NOR gates.
 - Design full subtractor using half subtractor and additional gates.
 - Convert following decimal number to Binary ,Octal, Hexadecimal and Gray code
 i) $(345)_{10}$ ii) $(818)_{10}$
- Q2. a) Explain collector to base bias Circuit with its stability factor. 10
 b) Minimize the following four variable logic function using K-map and Design using only NAND gates. 10
- $$f(A,B,C,D)=\sum m (0,1,2,3,5,8,9,10,11,12,14)$$
- Q3. a) Design 4-bit binary to gray code conversion using basic gates. 10
 b) i) Implement following using only one 8:1 Multiplexer and few gates.

$$F(A,B,C,D)= \sum m(1,3,4,5,8,9,12,15)$$

 ii) With neat logic diagram explain in short operation of Universal Shift Register. 10
- Q4. a) Design a Mod 10 synchronous counter using J-K Flipflop. 10
 b) Using Quine MC Cluskey Method determine Minimal SOP form for 10
- $$F(A,B,C,D)= \sum m(0,1,2,5,6,7,8,9,10,14)$$
- Q5. a) Explain about ENTITY declarations in VHDL and write VHDL program for NAND and OR gates. 10
 b) Implement 3 bit asynchronous u p counter and also sketch the timing diagram. 10
- Q6 Solve the following- 20
- Explain working of 8:1 Multiplexer.
 - Working of S-R flip flop(with its internal circuit diagram and truth table).
 - Explain working of Constant Current source.
 - Write VHDL program for full subtractor.