

(3 Hours)

(Total Marks : 80)

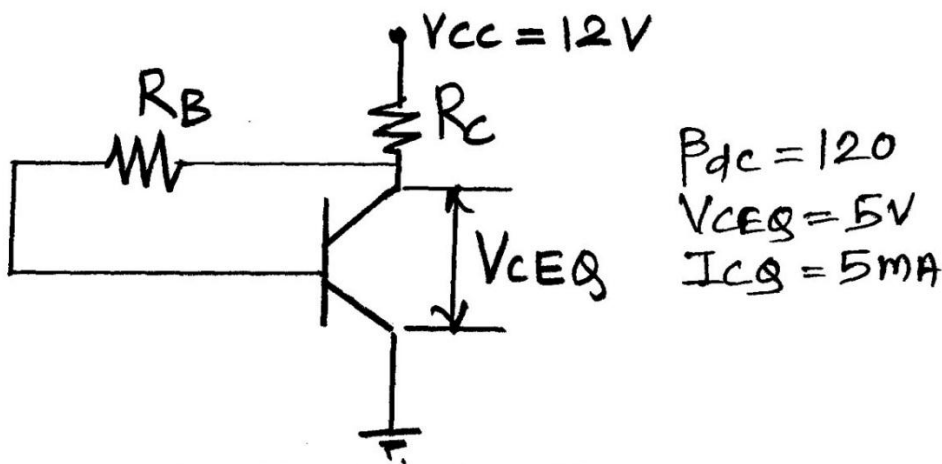
Please check whether you have got the right question paper.

- N.B.:**
- 1) Question No. 1 is compulsory.
 - 2) Solve any three questions from the remaining five questions.
 - 3) Figures to the right indicate full marks.
 - 4) Assume suitable data if necessary and mention the same in answer sheet.

1. Attempt any Four questions :

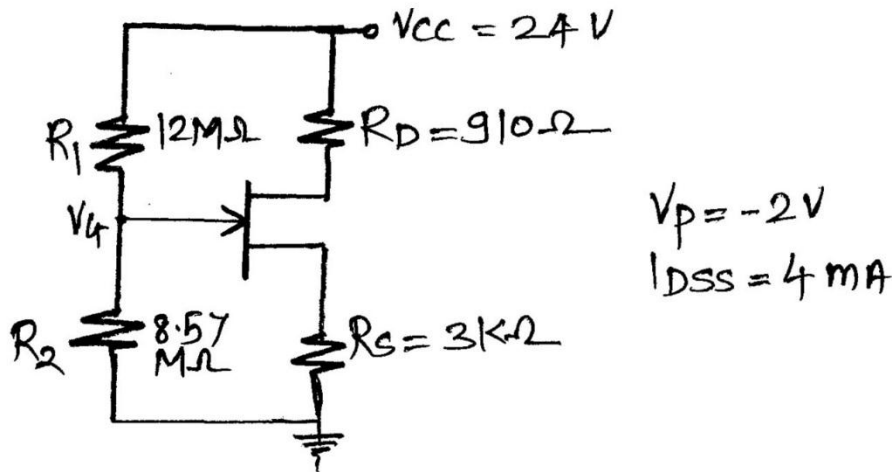
(20)

- a) Explain Various types of Resistors.
- b) Give the equation for the current in semiconductor diode. With the help of this equation explain in detail the V-I characteristics of a semiconductor diode.
- c) Explain Zener as a Voltage regulator.
- d) Find Values for R_B and R_C :

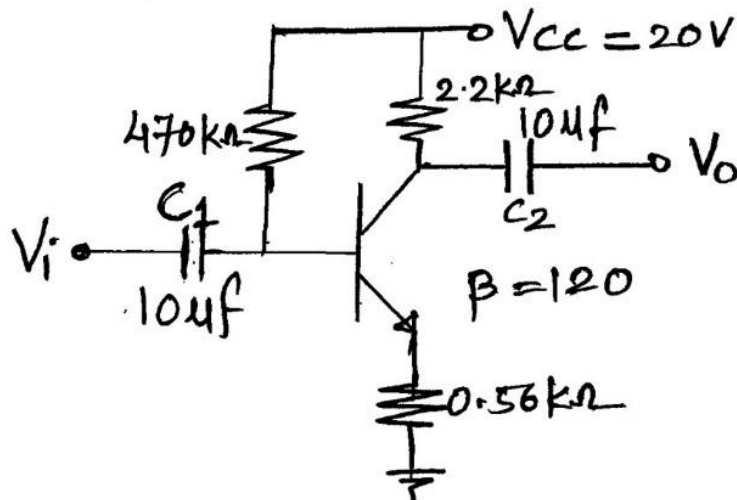


- e) Compare BJT CE Amplifier and JFET CS Amplifier.
 - f) Draw and explain high frequency model of BJT for CE configuration.
2. Design a single stage CE amplifier suitable for low frequencies up to 10Hz to give voltage gain A_v 70 and the output voltage of 4.5 Volts; employing transistor type BC147A. Calculate the expected A_v and maximum output voltage with negligible distortion that can be obtained from the designed circuit. Also, calculate the input resistance of the amplifier. Specify clearly the supply voltage V_{cc} for the designed circuit. (20)
3. a) A dc voltage of 350 Volts with peak ripple voltage not exceeding 5 Volts is required to supply a 500 Ω load. Determine following if inductor filter and full wave rectifier is used (10)
- 1) Inductance required
 - 2) Input voltage required.
- b) Explain and derive the expression for ripple factor for capacitor filter with full wave rectifier. (10)

4. a) For the circuit shown below determine I_{DQ} and verify if the FET will operate in pinch off region : (10)



- b) State and explain Miller theorem. (10)
5. a) Determine Z_i , Z_o and A_v for the circuit shown below : (10)



- b) Draw small Signal hybrid parameter equivalent circuit for CE amplifier and define the same. What are the advantages of h-parameters? (10)
- 6 Write short note on : (20)
- Hybrid Parameter
 - Regions of operation of FET
 - Stability factor of biasing circuits
 - DC load line concept in BJT. Why Q point should be at the middle of load line and fixed?

Transistor type	P _{max} @ 25°C Watts	I _{cm} @ 25°C Amps	V _{ce} ^{sat} volts	V _{ce} ^{sat} volts	V _{ce} ^{sat} volts	V _{ce} ^{sat} volts	V _{ce} ^{sat} volts	V _{ce} ^{sat} volts	D.C. current gain		Signal amp.	h _{FE} max.	Derate above 25°C W/°C
									min.	typ.			
2N 3055	115.5	15.0	1.1	100	60	70	90	7	200	20	15	120	1.8
ECN 055	50.0	5.0	1.0	60	50	55	60	5	200	25	25	125	1.5
ECN 149	30.0	4.0	1.0	50	40	—	—	8	150	30	33	115	3.5
ECN 100	5.0	0.7	0.6	70	60	65	—	6	200	50	50	200	1.2
DC147A	0.25	0.1	0.15	30	45	50	—	6	125	115	125	200	0.9
2N 525(PNP)	0.225	0.5	0.15	85	30	—	—	—	100	35	—	45	—
BC147B	0.25	0.1	0.15	50	45	50	—	6	125	200	240	330	0.9

Transistor type	h _{ic}	h _{oe}	h _{re}	θ _{jc}
BC 147A	2.7 K Ω	18 μ Ω	1.5 × 10 ⁻⁴	0.4°C/mw
2N 525 (PNP)	1.4 K Ω	25 μ Ω	1.2 × 10 ⁻⁴	—
BC 147B	4.5 K Ω	30 μ Ω	2 × 10 ⁻⁴	0.4°C/mw
ECN 100	500 Ω	—	—	—
ECN 149	250 Ω	—	—	—
ECN 055	100 Ω	—	—	—
2N 3055	25 Ω	—	—	—

BFW 11—JFET MUTUAL CHARACTERISTICS

-V _{GS} volts	I _D 0.0	I _D 0.2	I _D 0.4	I _D 0.6	I _D 0.8	I _D 1.0	I _D 1.2	I _D 1.6	I _D 2.0	I _D 2.4	I _D 2.5	I _D 3.0	I _D 3.5	I _D 4.0
I _D max. mA	10	9.0	8.3	7.6	6.8	6.1	5.4	4.2	3.1	2.2	2.0	1.1	0.5	0.0
I _D typ. mA	7.0	6.0	5.4	4.6	4.0	3.3	2.7	1.7	0.8	0.2	0.0	0.0	0.0	0.0
I _D min. mA	4.0	3.0	2.2	1.6	1.0	0.5	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0

N-Channel JFET

Type	V _{GS} max. Volts	V _{GS} max. Volts	V _{GS} max. Volts	P _D max. @ 25°C	T _J max.	I _D max.	I _D max.	I _D max.	I _D max.	I _D max.	I _D max.	I _D max.	I _D max.	I _D max.
2N3822	50	50	50	300 mW	175°C	2 mA	3000 μ Ω	6	50 K Ω	2 mW/°C	0.59°C/mW	—	—	—
BFW 11 (typical)	30	30	30	300 mW	200°C	7 mA	5600 μ Ω	2.5	50 K Ω	—	0.59°C/mW	—	—	—