(3 Hours) **[Total Marks : 80]**

Please check whether you have got the right question paper.

N.B.: **1)** **Question No.1 is compulsory.**
2) **Attempt any three questions from remaining.**
3) **All questions carry equal marks.**
4) **Assume suitable data wherever necessary.**

Q.1 Attempt **any four (04)** of the following: **20**

(a) Explain high frequency equivalent circuit of bipolar junction transistor (BJT).
(b) Write short note on the Cascode amplifier configuration.
(c) What are the advantages & disadvantages of negative feedback ?
(d) State & explain the Barkhausen's criterion.
(e) Describe what is cross-over distortion with a neat sketch.
(f) With neat sketch describe the V-I characteristics of DIAC.

Q.2 (a) Determine the lower & upper cut-off frequency (f_L&f_H) for the single stage common collector (CC) BJT amplifier asshown in Fig. 1 below. **10**

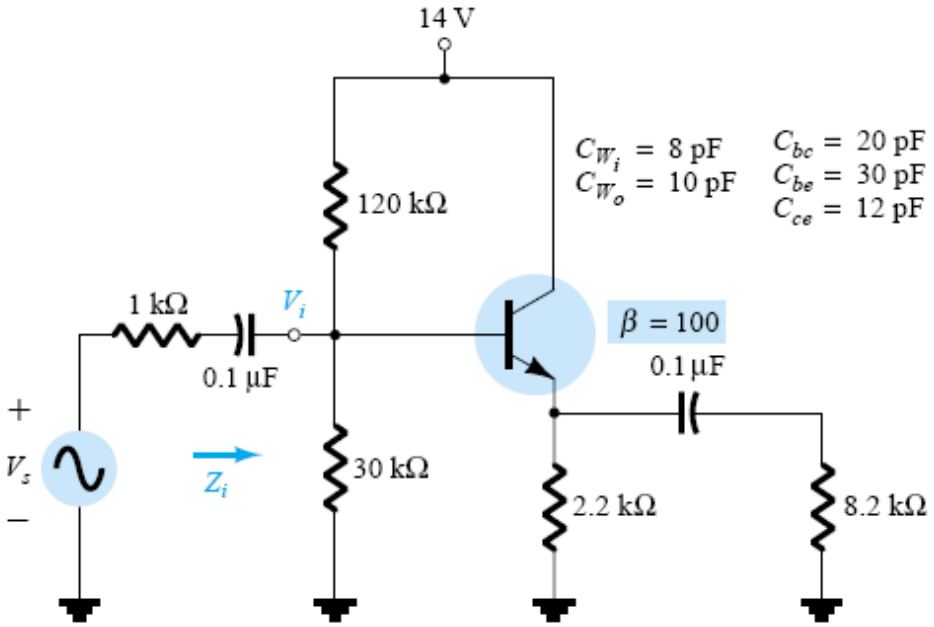

Fig. 1 – Common Collector (CC) BJT Amplifier for Q.2 (a)

Q.2 (b) Explain the high frequency response of CS – JFET amplifier with proper equations. Discuss the effects of various parasitic (inter-electrode & wiring) capacitances. **10**

Q.3 (a) Draw Class A transformer coupled amplifier & load line, derive the expressions for the maximum overall operating efficiency $\eta_{o(max)}$ & maximum collector conversion efficiency $\eta_{c(max)}$. **10**

Q.3 (b) Explain Class B push-pull amplifier with neat labeled diagram & derive the expressions for the maximum overall operating efficiency $\eta_{o(max)}$& maximum collector conversion efficiency $\eta_{c(max.)}$. **10**

Q.4 (a) For the E – MOSFET differential amplifier as shown in the Fig. 2:- **10**

(i) Determine the DC operating point (Q – Point)
(ii) Derive & calculate the differential mode gain (A_d)
(iii) Derive & calculate the common mode gain (A_c)
(iv) Calculate the common mode rejection ratio (CMRR)

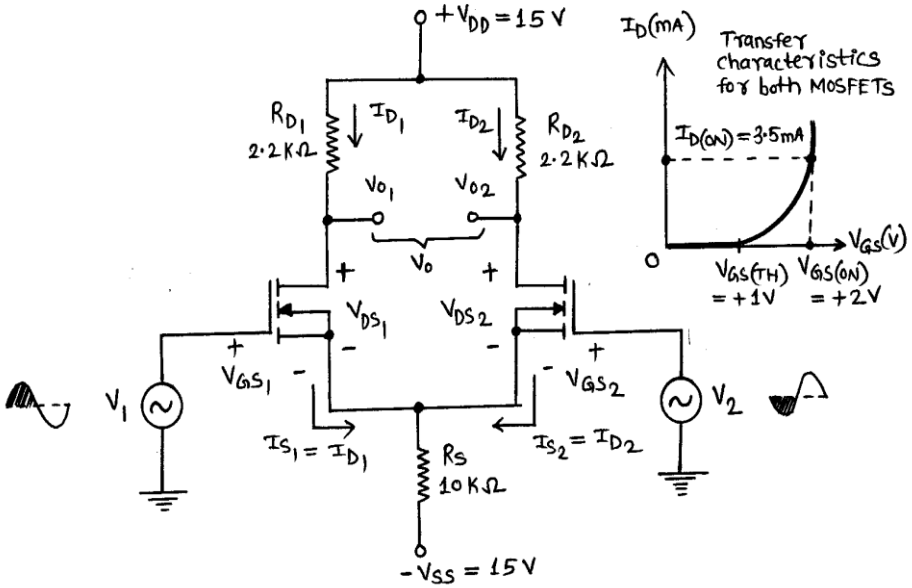

Fig. 2 – The E – MOSFET Differential Amplifier for Q.4 (a)

Q.4 (b) Identify the negative feedback topology as shown in the Fig. 3 below. Analyze to derive the expressions for the input resistance with feedback (R_{if}) & output resistance with feedback (R_{of}). **10**

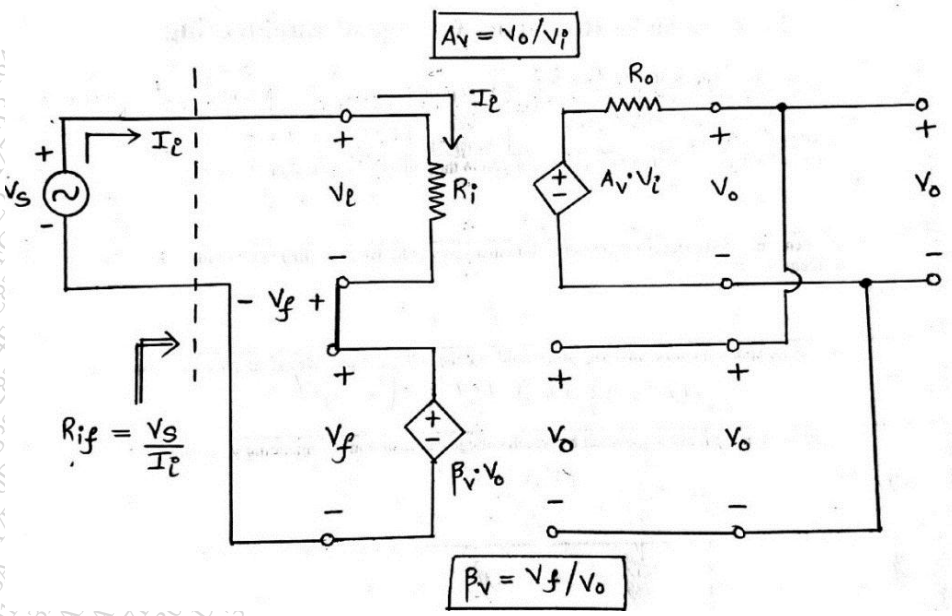

Fig. 3 – Negative Feedback Amplifier Topology for Q.4 (b)

Q.5 (a) With a neat labelled diagram, explain the Hartley oscillator. Describe its advantages & disadvantages. Design the same for 50 kHz. **10**

Q.5 (b) Identify the low frequency RC oscillator from the Fig. 4 & explain its working with its advantages & disadvantages. From the given component values, calculate output frequency of oscillations (f_o). **10**

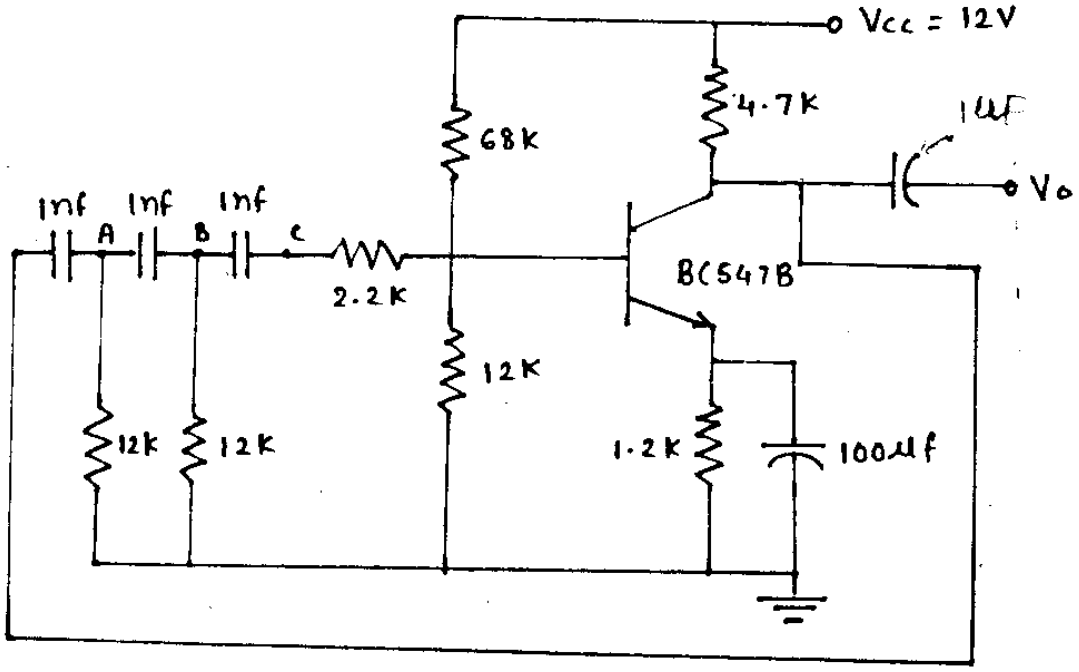

Fig. 4 – The low frequency RC oscillator for Q.5 (b)

Q.6 (a) Explain the working of silicon controlled rectifier (SCR) using the two-transistor analogy with a neat labelled diagram. Draw the structure / construction & V-I characteristics of SCR. **10**

Q.6 (b) Describe construction & explain the working of uni-junction transistor (UJT) with neat labelled diagram & V-I characteristics. Define the term 'intrinsic stand-off ratio'. **10**
