

(3 Hours)

Max Marks: 80

N:B:

1. Question No. 1 is compulsory.
2. Out of remaining questions, attempt any three questions.
3. Assume suitable additional data if required.
4. Figures in brackets on the right hand side indicate full marks.

- Q.1** a) Perform following subtraction using 2's compliment. [5]
 i) $(44)_{10} - (66)_{10}$ ii) $(76)_{10} - (34)_{10}$
 b) Define Noise margin, Propagation delay and Power dissipation. [5]
 c) Compare combinational circuits and sequential circuits. [5]
 d) Compare TTL and CMOS logic. [5]
- Q.2** a) Simplify following expression using K-map and implement using only [10]
 NOR gates. $F(A,B,C) = \sum m(1,4,5,6,7)$
 b) Convert D flip flop to T flip flop. [05]
 c) Explain race around condition in JK flip flop. [05]
- Q.3** a) Minimize the following expression using Quine McClusky Technique [10]
 $F(A,B,C,D) = \sum m(2,3,6,7,8,9,13,15)$
 b) Design full adder using logic gates. [10]
- Q.4** a) Design mod-10 ripple up counter using JK flip flop. Draw its timing [10]
 diagram.
 b) Implement the following function using single 8:1 Multiplexer and logic [10]
 gates. $F(A, B, C, D) = \sum m(0,1,2,4,5,6,8,9,10,12,13,15)$.
- Q.5** a) Explain the various features of VHDL and its modelling style. [10]
 b) Design mod-5 synchronous up counter using T flip flop. [10]
- Q.6** a) Write short note on FPGA. [10]
 b) What is shift register? Explain any one type of shift register. [10]