Q. P. Code: 25637

Time: 3 hours Marks: 80

N.B : (1) Question No.1 is compulsory.

(2) Attempt any three questions from remaining questions.

(3) Figures to the right indicate full marks.

Q1(a)Draw register structure of IA-32 family 5

(b) Compare RISC and CISC architectures. 5

(c) Explain restoring division algorithm and draw its flowchart. 5

(d) Compare paging and segmentation. 5

Q2(a)Explain any one hardwired technique of control unit design. 10

(b) Explain various modes of DMA transfer. 10

Q3(a)Explain the advantages of pipelining. Explain various types of pipeline hazards and their solutions. 10

(b)Explain various architectures of cache memory. 10

Q4 (a)Explain various page replacement policies. 10

(b)Explain the structure of serial and parallel ports. What are the methods to access it? 10

Q5 (a) What is virtual memory ?Explain how paging is useful in implementing virtual memory. 10

(b)Explain execution of a complete instruction with details. How are branch instructions executed? 10

Q6(a)What are different addressing modes of IA-32 family? Explain with examples. 10

(b) Explain single bus and multiple bus organization. 10

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