Duration:3 hrs **Maximum Marks :80**

Note: 1.Question 1 is compulsory.

2.Solve any three out of remaining .

3.Assume suitable data if necessary

4.Draw proper diagrams

Q.1. Solve any four.

(a) Explain briefly about transfer characteristics of CMOS inverter. [5]

(b) Design a 4:1 MUX using NMOS transmission gates. [5]

(c) Implement two I/P NOR gate using CMOS inverter and Pseudo NMOS Logic. [5]

(d) Compare Ripple carry adder with Carry Look Ahead adder. [5]

(e) Compare ROM and RAM. [5]

Q.2 (a) Explain different inverter circuits and compare their performance .What is the benefit of using active load? [10]

(b) Compare the full scaling model with constant voltage scaling model for MOSFETS. Demonstrate clearly the effects of scaling on the device density, speed of the circuit, power consumption and current density of the gates [10]

Q.3 (a) Implement JK FF using Static CMOS. What are other design methods for it? [10]

(b) Explain Read Write operation of 6-T SRAM cell in detail. [10]

Q.4 (a) What is ESD protection? Explain with example. [10]

(b) How multiplication operation is carried out**?** Explain with example. [10]

Q.5 (a) What is importance of Global and Local clock? Explain different clock distribution schemes? [10]

(b) What is NOR based ROM and NAND based ROM? Hence explain any one decoder. [10]

Q.6 Write short notes on (any three) [20]
(a) Programming techniques used for EEPROM
(b) Array Multiplier
(c) CMOS latch-up and its prevention
(d) Interconnect scaling and RC delay

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