

(3 Hours)

[Total Marks: 80]

- N. B. : (1) Question No. 1 is compulsory.
 (2) Attempt any three out of remaining.
 (3) Assume suitable data wherever required.

Q.1 Solve the following (**Any four**)

[20]

- A. What is the significance of 'scope resolution operator'.
- B. Justify if code coverage is 100%, it indicates verification is done 100%.
- C. Short note on mailbox and describe their use in System Verilog with suitable example.
- D. Explain the concept of an interface with suitable example and why it is used?
- E. Draw layered test bench block diagram mentioning each layer clearly.

Q.2 A. Draw the architecture of FPGA and specify its important components. Highlight the features of Virtex – 7.

[10]

B. Explain the concept of Switch level modelling. Write Verilog code for 2:1 mux using Structural modelling.

[10]

Q.3 A. Discuss Silicon challenges considering time closure, capacity, physical properties, design productivity gap and time to market.

[10]

B. [10]

i. Create an unpacked array, 'my_array', containing 4 elements of user defined type.

ii. Initialize it to 4'hA, 4'hB, 4'hC, and 4'hD.

iii. Stream my_array into **my_array_s**, right to left on a bit basis and print out **my_array_s**.

iv. Given the following code, determine what will be displayed.

```
module test;
string students[$]={"Austin", "Noel", "Gary"};
initial begin
    $students.insert(2,"Sakshi");
    $display("students[2]=%s", students[2]);
    $students.pop_front("Swapnaja");
    $display("students[2]=%s", students[2]);
    $display("size=%d", students.size);
    $display("push back=%s", students.push_back);
    $display("size=%d", students.size);
end
endmodule
```

```
class Transaction;
    rand opcode_e opcode;
    rand byte operand1;
    rand byte operand2;
endclass
```

1. The opcode shall take on the values ADD or SUB (Use 1 coverage bin).
2. The opcode shall take on the values ADD followed by SUB.
3. Opcode must not equal DIV" (hint: report an error using illegal_bins).