



ATHARVA EDUCATIONAL TRUST'S
ATHARVA COLLEGE OF ENGINEERING

(Approved by AICTE, Recognized by Government of Maharashtra
& Affiliated to University of Mumbai - Estd. 1999 - 2000)

Department of Electronics and Telecommunication Engineering

Report For
Webinar
on
“VLSI Technology”

Dated : Thurs, November 25th 2021.

Schedule: 2:00 to 3:00 pm

Coordinators: Prof. Joslyn Gracias, Prof. Ruchi Chauhan
Assistant Professor, EXTC Dept, ACE

Details of the Speaker:

Sr. No.	Name of Speaker	Industry	Designation	Session	Audience	Meet link
1.	Prof Anup Dinkar Taryalkar	Academician, Atharva College of Engg	Assistant Professor	2:00 to 3:00 pm	SE Students EXTC	https://meet.google.com/bde-xmpd-bhc

Objective of Webinar:

The main objective of the webinar was to provide an overview of the fundamental principles of VLSI, ASIC / FPGA design and analyze the basic building blocks of large-scale digital integrated circuits.

Content:

- Introduce VLSI field to participants
- Exposure to FPGA's
- Introduction to Hardware description Languages
- Discussion on implementations of mini projects

Brief Description:

The Electronics and Telecommunication Engineering Department of Atharva College of Engineering in association with IETE student forum- ACE, successfully organized a one hour Webinar on “VLSI Technology” through online platform Google Meet .

The event started with a Welcome address by student host Amitesh Sangla of SE EXTC. He invited the I/c HOD-EXTC Prof. Mahalaxmi Palinje to share her thoughts on the selected webinar topic. Thereafter, the student host introduced the profile of session speaker to the participants and handed over the session.



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The speaker delivered an excellent session by introducing VLSI field to students. Insights on FPGA's and Hardware Description Languages were given. Speaker also discussed the implementation of mini projects in VLSI field.

Queries of the students were resolved by speaker after the session. Vote of Thanks was given by Ms. Simran Singh, SE EXTC.

Outcome:

1. Participants were exposed to history and basics of VLSI. They were given an overall idea of the technology.
2. The session helped the participants to analyse the basic building blocks of large-scale digital integrated circuits and created awareness on job opportunities in Indian semiconductor and electronic systems industry outside of the generic 'IT' umbrella.
3. The session created an awareness selecting the mini projects based on interested domain to enhance the performance.

No of Participants: 87

Photo Gallery:





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The screenshot shows a Google Meet interface with a presentation slide titled "STEPS REQUIRED TO BE A VLSI ENGINEER:". The slide lists four requirements:

- a. Good knowledge of Digital Electronics
- b. Good knowledge of Programming (Basic C programming)
- c. Verilog System Verilog
- d. Projects

The meeting participants visible are Anup Taryalkar, VISHAL SANAP, ANKUSH ATHAWALE, and Abdul Kabeer. The session is titled "Session by Prof. Joslyn Gracias" and the time is 2:53 PM on 11/25/2021.

The screenshot shows a Google Meet interface with a presentation slide titled "COMPANIES OF VLSI". The slide lists eight companies:

1. Intel
2. NVIDIA
3. Qualcomm
4. Broadcom
5. TI (Texas Instrument)
6. ARM
7. Xilinx
8. AMD

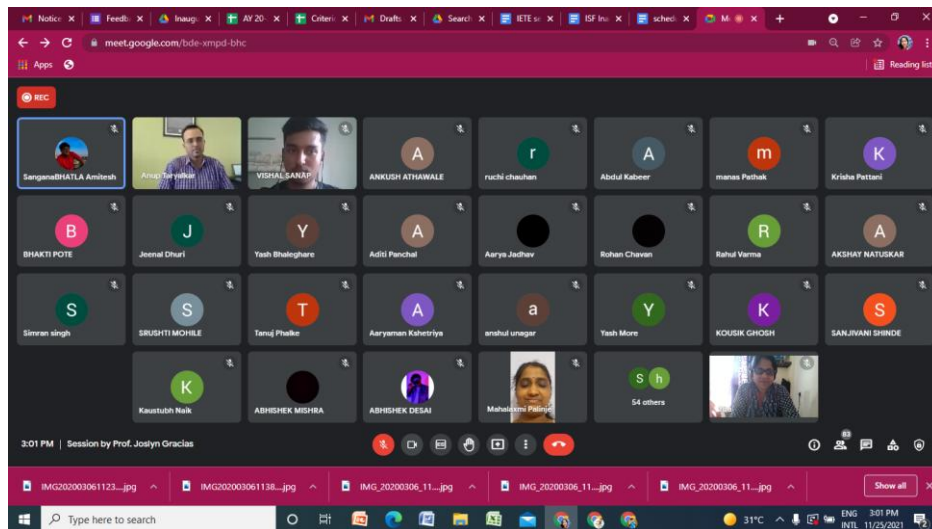
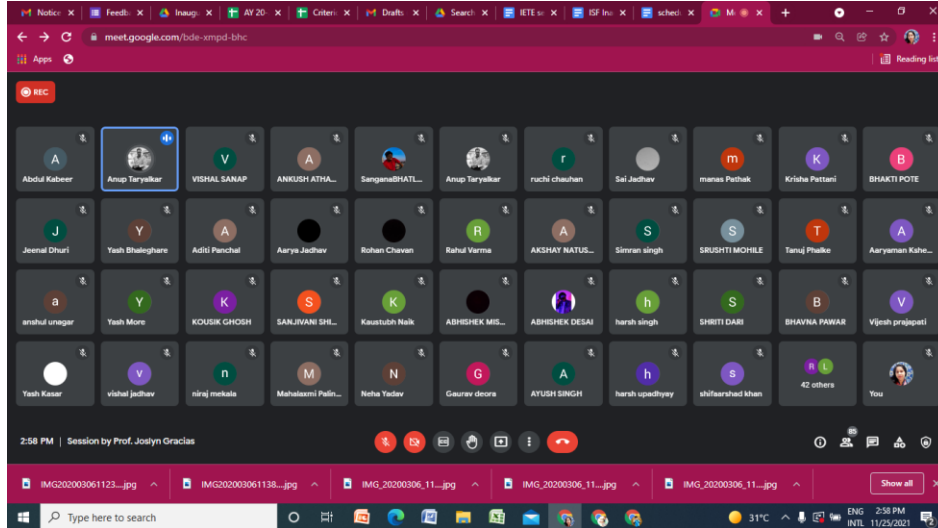
The meeting participants visible are Anup Taryalkar, VISHAL SANAP, ANKUSH ATHAWALE, and Abdul Kabeer. A notification for "schedule for iete inauguration 6 March 2020.docx - Google Docs" is visible in the top right. The session is titled "Session by Prof. Joslyn Gracias" and the time is 2:56 PM on 11/25/2021.



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Prof. Joslyn Gracias
Prof. Ruchi Chauhan
(Webinar Coordinator)

Prof. Mahalaxmi Palinje
I/C HOD, EXTC
EXTC DEPT, ACE